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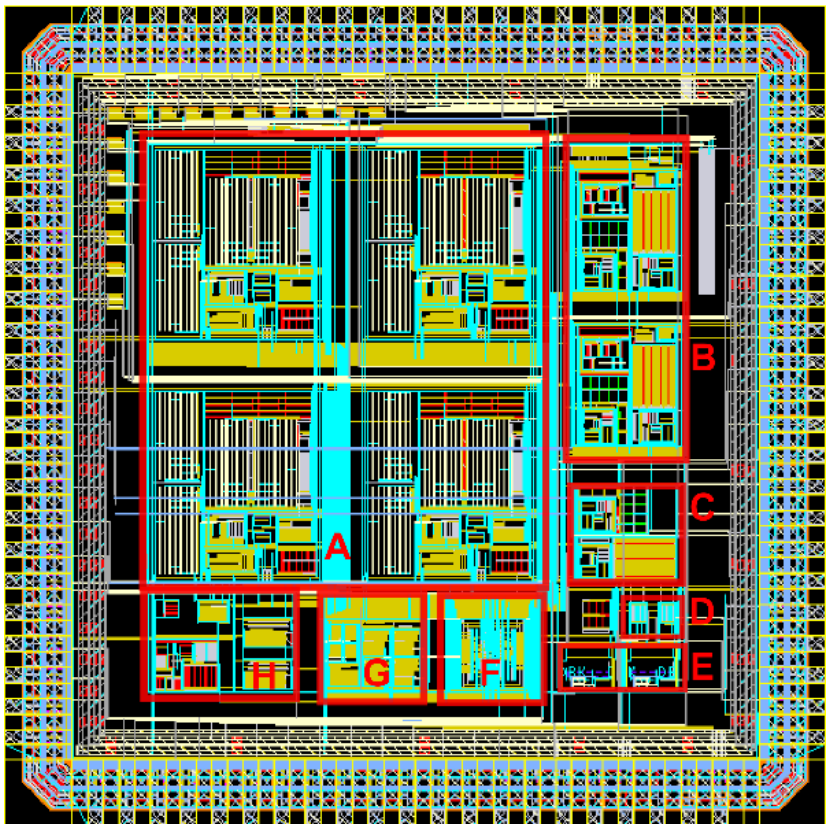
#11, 1st Floor, JCR Tower, Anatha Ram Reddy Layout, Marathalli, Bangalore, KA-560037

ADVANCED VLSI COURSE
IN
ANALOG LAYOUT DESIGN

Course covers all advanced topics as prescribed by industry requirements



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COURSE SYLLABUS

In this course we use 65nm and 28nm, 14nm technology nodes.

All modules are covered in details from basic to advanced topics with practical implementations.

Course Syllabus:

Module 1: Introduction to Analog circuit and Layout design

- Basics of analog circuit design concepts
- Analog circuit design challenges and implementation strategies
- Introduction to Analog layout concepts
- Layout design rules and process

Module 2: IC Fabrication flow

- Introduction to fabrication techniques
- Ionization and wafer technology
- CMOS/BJT/MOSFET/FINFET IC fabrication steps
- Fabrication techniques for Deep submicron technology

Module 3 : Introduction to Analog layout concepts

- Understanding various mask layers
- Layout requirements for each layers
- Layout floor planning
- BUMP/PAD/ESD/PIN planning

Module 4: Introduction to Layout editor tools

- Creating libraries, adding and managing layout cell views
- Creating config views for DRC/LVS checks
- Layout editor tool commands and shortcuts
- Commands for creating netlist from schematics and exporting to layout view
- Layout spice simulation commands

Module 5: Standard Cell Layout design

- Layout of basic CMOS gates, INV, AND, NAND, OR, NOR
- Complex cell layout design

Module 6: Layout or Discrete components

- BJT, DIODE, Clamp cell designs
- Resister, Capacitors, Inductors design
- BiCMOS logic designs

Module 7: Layout Design Techniques

- Orientations
- Multifingers/common Centriod/Quads
- Distance/Gaps between layout layers
- Overlaying and Adjacent layers
- Same Area/Perimeter ratios
- soft edge shapes

Module 8: Layout Design Checks

- DRC/ERC/LVS soft checks
- Electro migration checks and Removal techniques
- IR Drop analysis
- Antenna affect checks and Removal techniques
- SI checks like crosstalk and EMI issues
- ESD checks and ESD cell designs
- Dish effects checks and removal
- Well proximity checks

Module 9: Analog Layout Designs

- Analog Amaplifiers, comparators, filters circuits
- Opamp sense amplifier designs
- Differential Opamp Designs
- Bandgap layout Designs
- BUMP/ESD/Gaurd ring designs
- Tap Cell Designs

Module 10: Memory Layout Designs

- SRAM cell design
- Rows and Columns Decoders
- Sense Amplifier design
- Write/read control logic
- Power supply design
- Dual port RAM cell designs

Module 11 : Final Project

- PLL, LDO, ADC layouts. In 65nm, 32nm, 14nm
- Assignments given for Lab practice

Prerequisites:

With Electronics major subject in B.E/B.Tech/M.E/M.Tech, atleast 60% throughout academic career Basic knowledge in Electronic Design circuits, CMOS fundamentals. Good logical & analytical ability

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Admission procedure:

Selection based on Academic merit and personal Interviews for eligible interested Candidates. Please walkin/mail/call us to schedule for personal interview. Outstanding performers will get special concessions in Fees. Working VLSI/Software professionals will get direct admissions.

Grading & Certifications

All the participants who fulfilled course assignments, projects, topic wise exams would be awarded with **Course completion Certification**

Placement Assistance

All the eligible candidates who have fulfilled requirements of the course will be given 100% placement assistance.

Duration:

4 months full time regular weekly & weekend batches

Course Fees:

90,000/-