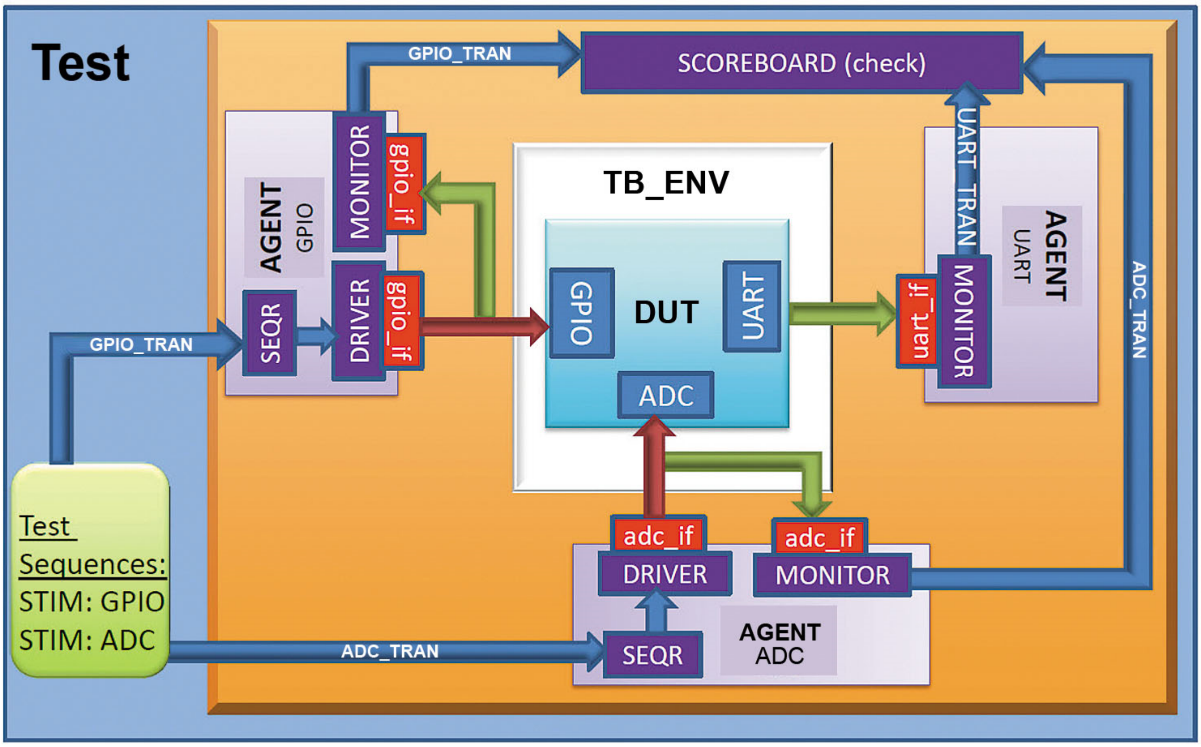
ADVANCED VLSI DESIGN VERIFICATION USING SYSTEMVERILOG & UVM

Course covers all advanced topics as prescribed by industry requirements



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Overview of Systemverilog & UVM

SystemVerilog is a major extension to Verilog-2001, adding significant new features to Verilog for verification, design and synthesis. Enhancements range from simple enhancements to existing constructs, addition of new language constructs to the inclusion of a complete Object Oriented paradigm features. There are also considerable improvements in the usability of Verilog for RTL design.

Overview

NEOSCHIP's *Verification Using SystemVerilog* course gives you an in-depth introduction to the main enhancements that SystemVerilog offers for testbench development, discussing the benefits and issues with the new features. It also demonstrates how verification is more efficiently and effectively done using SystemVerilog constructs. The course explores in depth verification enhancements such as object-oriented design, constraint random generation, and functional coverage.

Objectives

- To explore the new features of SystemVerilog for verification and demonstrate the improvements in verification environment efficiency from their use.
- To explain key features for verification, such as classes, OOP, randomization, and functional coverage and illustrate how to exploit these features for more efficient verification and testbench development.

Duration: 4 Months

Prerequisites:

Attendees must be familiar with Verilog and ideally, but not essentially, Verilog2001. No prior knowledge of SystemVerilog is required. If you have queries on these prerequisites, please contact neoschip technologies.

Table of Contents

Module 1

Introduction to Verification Languages

Verification Tools

- Source Debugging Tools.
- Code Coverage Tools.
- Functional/Assertion Coverage Tools.

Verification Process in ASIC Flow

- Functional Verification Process.
- Test Plan Development.
- TestBench Development
- Testcase Development.
- Behavioral Models Development.
- BFM's Developments.
- Monitors Development.
- Checker Development.
- Functional group & Assert group Development using OVL & SVA.
- Module/Block/Chip Level Verification.
- Coverage driven Random Verification.
- Verification Metric Analysis (Code & Function coverage analysis).

Timing Verification Process.

- Zero-Delay Gate-Level Verification.
- SDF-Annotated Gate-Level Verification.
- Timing Verification Process.
- Introduction to Formal Verification.
- Introduction Power-Aware Verification.
- Introduction to co-simulation verification.
- Introduction to AMS Verification.

- Introduction to Physical Verification.

Test-Bench Automation

- Introduction to Scripting using Perl.
- Linux/Unix Utilities.
- FTP.
- Telnet.
- Version Management.
- Bug Tracking.

Module 2

Introduction to SystemVerilog

- Language evolution
- SV Design
- SV Assertions
- SV testbench
- DPI
- API

Abstract modeling constructs

- Data types, type checking, type cast
- Structure and union
- Packages

- Enhanced always, case/if... else, loop, flow
- Operators
- Arrays and its operators
- SV scheduling semantics
- DUT description
- Interface
- Grouping signals
- Modport
- Clocking block, skews
- Tasks, functions
- Transaction Level Modeling (TLM)

Systemverilog Class

- Object Oriented programming (OOP's)
- Type cast
- inheritance
- polymorphism
- parameterization
- new constructor
- Automatic garbage collection
- Virtual interface
- task and function
- automatic and static functions (void & extern)
- Argument pass by value/reference

- Program construct
- Final block
- Enhanced Concurrency modeling
- Threads – variants of fork .. join, Disable fork, terminate

Inter process communication

- Events
- semaphore
- mailboxes
- queues

Module 3

Random vs. directed testing

- Need for random testing
- Constraints in SVTB
- Class constraint
- Randomize success / fail
- Inheritance Randomize.with()
- Distribution
- Function calls in constraints
- Array constraints
- Pre / post randomize

Functional coverage

- Motivation for SV Coverage Driven verification
- Introduction to SV coverage
- Types of coverage
- Functional coverage process
- Covergroup
- Coverpoint
- Concept of binning
- Cross Coverage
- Sampling event

DPI

- Import DPI
- Export DPI
- DPI Context
- DPI vs. VPI/PLI

Module 4

UVM Based verification

- Overview of different verification methodologies
- Evolution of Verification methodologies
- Migration of OVM to UVM
- Introduction to UVM

- Verification phasing
- Reporting
- Transactions
- Test bench Configuration
- TLM Basics
- Events, Sequence, Sequencer and Driver
- Virtual Sequences
- Monitor & Subscriber
- Agents
- UVM Environment
- Test bench classes
- Callbacks
- Coverage
- Register layer

Module 4

Industry standard project: (Select any one)

- AHB Master/slave
- AXI Master/Slave
- AHB-I2C
- AHB Uart
- AHB Memory controller.
- Microcontrollers/DSP processors

- DDR2
- Ethernet
- AXI Master/Slave

Prerequisites:

With Electronics major subject in B.E/B.Tech/M.E/M.Tech, atleast 60% throughout academic career Basic knowledge in Verilog/VHDL Good knowledge on Digital design Good knowledge on any Microcontroller/Processor architectures Good logical & analytical ability

Admission procedure:

Selection based on written test and personal Interviews for eligible interested Candidates. Syllabus for written test covers Digital logic design, Processor architecture, and Analytical and Logical questions. Please walkin/mail/call us to schedule for written test & personal interview. Outstanding performers will get special concessions in Fees. Working VLSI/Software professionals will get direct admissions.

Grading & Certifications

All the participants who fulfilled course assignments, projects, topic wise exams would be awarded with Course completion Certification

Placement Assistance

All the eligible candidates who have fulfilled requirements of the course will be given 100% placement assistance.

Duration:

4 months full time regular weekly & weekend batches

Course Fees:

79,000/- Plus Taxes