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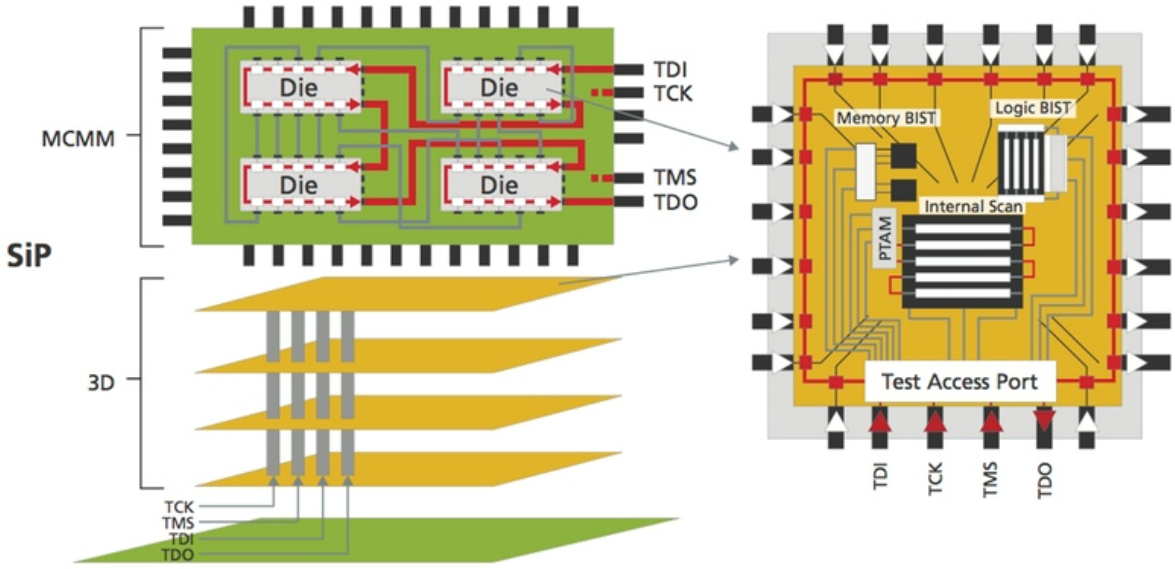
Advanced VLSI Course In DFT Design

Course covers all advanced topics as prescribed by industry requirements



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COURSE SYLLABUS

In this course we use 180nm, 90nm, 45nm and 28nm technology nodes.

All modules are covered in details from basic to advanced topics with practical implementations.

Module-1: Introduction to VLSI Digital Design

Overview of Digital design methodology, Representations of Digital Design and understanding of digital systems, logic gates, combinational and sequential logic. Review HDL's and RTL implementation of digital logic systems.

Module-2: Semiconductor technologies and CMOS fundamentals

Introduction to semiconductor technologies, logic gates, Review CMOS basics, CMOS digital design concepts and understanding CMOS process parameters and characterization of logic gates.

Module-3: Linux OS and TCL Scripting

Linux OS Syllabus

- Introduction to the Linux Operating System
- How to Download & Install Linux (RHEL/CentOS) in Windows
- Linux vs Windows: What's the Difference?
- Linux Command Line Tutorial: Manipulate Terminal with CD Commands
- Basic Linux/Unix Commands with Examples
- File Permissions in Linux/Unix with Example
- Input Output Redirection in Linux/Unix Examples
- Pipe, Grep and Sort Command in Linux/Unix with Examples
- Linux Regular Expression Tutorial: Grep Regex Example

TCL Scripting Syllabus

- Introduction and Overview
- Tcl Syntax: quoting and substitution
- Expressions
- Variables: simple variables; associative arrays
- Lists; Keyed Lists
- Control Structures: built-ins
- Procedures; Recursion
- The Unix File System
- Files and I/O
- Strings
- Regular Expressions
- Writing Applications; Auto loading; Timing; Profiling
- Processes
- Error Handling; Defining Control Structures; Exceptions

- Client / Server; Distributed Programming
- Expect

Module-4: ASIC design flow and Design for Testability

Overview of ASIC/SOC design flow, Digital Design Concepts and Introduction to design faults that occur during chip design. Understanding stuck at faults, transition faults, coupling faults, pattern sensitive faults, and dynamic faults.

Module-5: Introduction To Design For Testability

- DFT fundamentals
- Need for DFT in chip design
- Understanding fabrication flows and challenges
- ATPG basics

Module-6: DFT Scan requirements

- Observability and Controllability
- DFT Scan logic design
- DFT Design rules
- Scan register vs normal registers
- Scan chains & Scan pipelines
- Scan Insertion techniques
- Scan protocol design

Module-7: Block level & SoC level DFT design

- DFT flows and process steps
- Defining DFT scan constraints
- DFT synthesis and review scan protocols
- DRC Checks (DFT Rule Checks)
- DRC Error reporting and categories
- Over view of block level & SoC level DFT scan design

Module-8: DFT Scan Design

- Scan Chain Architecture
- Mux-D Scan Design
- Clocked Scan Design
- Level Sensitive Scan Design(LSSD)
- Enhanced Scan Design
- Low-Power Scan Design

Module-9: Introduction Logic BIST

- BIST Controllers
- BIST Test Pattern Generators

- Test pattern compaction
- BIST Architectures
- Test Per Scan BIST
- Test Per Clock BIST
- STUMPS based BIST Architecture
- CBILBO BIST Architecture
- Coverage Driven Logic BIST
- Low Power BIST

Module-10: DFT Scan Insertion

- Scan Synthesis flows
- DFT tools and setup for scan insertion
- Scan Constraints and protocol definitions
- Setting ATE configuration
- Scan Specifications
- Pre and Post Scan checks
- Identifying Scan Chains and Estimating Test Coverages
- Scan DRC(DFT rule checker) checks
- Scan Chain optimization

Module-11: DFT Scan Violations and Fixes

- Scan Issues with various design scenarious
- Gated clocks and clock muxes, Clock Generators
- Controllability of Asynchronous logic, resets
- Scan Design initialization sequence
- Scan Capture problems due to clock skews
- Scan buffers, Shift registers, tristate & bidirectional ports
- Latch based designs and combinational loops

Module-12: Advanced DFT Design concepts

- Scan chain insertion with Clock mixing and no mixing
- Mixing clock edges, clocking on both edges
- Internal clock domains
- Lockup latch
- Custom Scan paths
- Scan in/out port sharing techniques

Module-13: DFT Scan compression techniques

- DFT Scan compression with limited scan pins
- Scan Serializer and Deserializer
- Block level and Chip level compression techniques
- External and Internal clock usage for serializer and Deserializer clocks

- Adaptive scan techniques

Module-14: DFT BIST Architecture

- BIST Architecture
- Logic BIST
- Memory BIST
- RAM BIST
- ROM BIST
- Memory models
- Memory Faults
- Stuck open and short faults
- Coupling faults
- Pattern sensitive faults
- Read Disturb faults
- Dynamic faults, recovery faults retention faults
- March Tests
- Word oriented march tests
- Inter and Intra word tests
- Word coupling faults tests
- MISR

Module-15: Test Pattern Generation using ATPG flows

- Design Tools
- ATPG tools and setup
- ATE tools
- STIL patterns(Defines Test protocols, Test pattern and Test timing)
- Build Mode, DRC Mode and Test Mode

Module-16: ATPG pattern generation concepts

- ATPG pattern generation constraints
- Analyzing DFT rule violations
- ATPG coverage estimation
- ATPG STIL pattern generation
- Dynamic and Static Pattern compression techniques
- Review results Detectable and undetectable faults

Module-17: ATPG Fault modeling and simulations

- Fault Simulation with functional patterns
- Fault Grading for functional simulations
- Design Verification setup with ATPG fault model simulations
- Memory modeling for ATPG simulations

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Module-18: Final Project

Project on Block level and SoC level DFT insertion and ATPG generation with fault model simulations

Prerequisites:

With Electronics major subject in B.E/B.Tech/M.E/M.Tech, atleast 60% throughout academic career Basic knowledge in Verilog/VHDL Good knowledge on Digital design Good knowledge on any Microcontroller/Processor architectures Good logical & analytical ability.

Admission procedure:

Selection based on written test and personal Interviews for eligible interested Candidates. Syllabus for written test covers Digital logic design, Processor architecture, and Analytical and Logical questions. Please walkin/mail/call us to schedule for written test & personal interview. Outstanding performers will get special concessions in Fees. Working VLSI/Software professionals will get direct admissions.

Grading & Certifications

All the participants who fulfilled course assignments, projects, topic wise exams would be awarded with Course completion Certification.

Placement Assistance

All the eligible candidates who have fulfilled requirements of the course will be given 100% placement assistance.

Duration:

4 months full time regular weekly & weekend batches

Course Fees:

Rs: 70,000/- (Inc GST)