NeosChip Semiconductors
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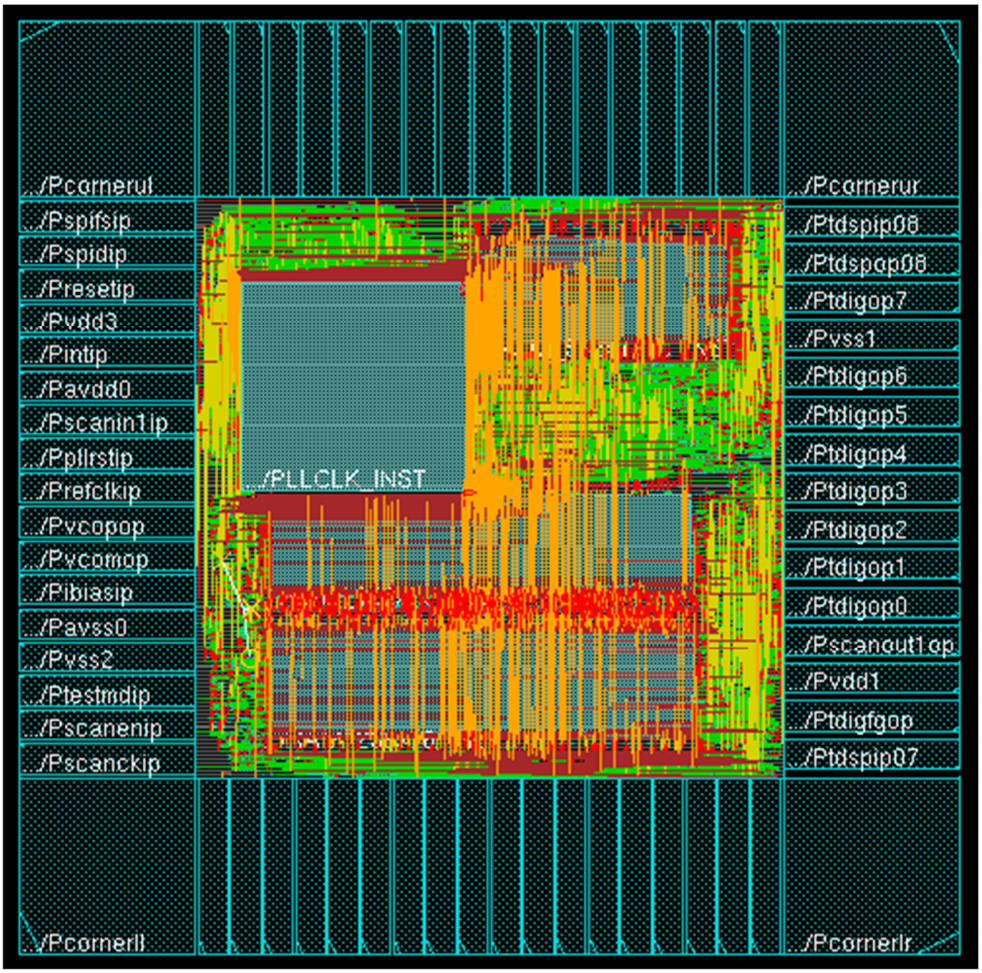
#11, 1st Floor, JCR Tower, Anatha Ram Reddy Layout, Marathalli, Bangalore, KA-560037

VLSI PHYSICAL DESIGN

Course Brochure

Course covers all advanced topics as prescribed by industry requirements



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COURSE SYLLABUS

In this course we use 180nm, 90nm, 45nm and 28nm technology nodes.

All modules are covered in details from basic to advanced topics with practical implementations.

Module-1: Introduction to VLSI Digital Design

- Overview of Digital design methodology,
- Representations of Digital Design and understanding of digital systems,
- Digital logic gates and logical operations
- Combinational and sequential logic.
- Review HDL's and RTL implementation of digital logic systems.

Module-2: Semiconductor technologies and CMOS fundamentals

- Introduction to semiconductor technologies,
- TTL, Domino, Dynamic and CMOS logic gates,
- Fundamentals of CMOS circuits,
- CMOS digital design concepts.
- Understanding CMOS process parameters and characterization of logic gates.

Module-3: ASIC design flow and design planning

- Overview of ASIC/SOC design flow,
- Digital Design Concepts and Physical Design flow setup.
- Review of ASIC fundamentals & fabrication methodologies.

Module-4: ADVANCED DIGITAL DESIGN

- Introduction to digital design
- Number representation, complements and Boolean logic
- Basic logic gates and logic functions
- Optimization techniques for logic functions
- Design of combinational circuits.
- Implementation and analysis of combinational circuits like, adders, comparator, multiplier etc.
- Design of synchronous sequential circuits.
- Implementation and analysis of sequential circuits Flip-Flops, registers, counters, and simple processor
- Design of Asynchronous Sequential Circuits
- Design of Finite State Machines (FSM)

- Discussion - Special circuits like LFSR, FIFO, barrel shifter etc.
- Case study – PROTOCOLS LIKE AHB, APB, PCI, UART etc.

Module-5: VERILOG HDL

- Introduction to Verilog HDL.
- Gate-Level modeling.
- Dataflow modeling.
- Operators.
- Data types.
- Modeling timing and delays.
- Behavioral modeling.
- Parameters, tasks and functions.
- Compiler directives.
- System tasks.
- File input/output.
- Switch-level modeling.
- User Defined Primitives.
- Design examples – FSM, ALU, RAM, ROM, UART, Traffic light signal.

Module-6: Linux OS and TCL Scripting

Linux OS Syllabus

- Introduction to the Linux Operating System
- How to Download & Install Linux (RHEL/CentOS) in Windows
- Linux vs Windows: What's the Difference?
- Linux Command Line Tutorial: Manipulate Terminal with CD Commands
- Basic Linux/Unix Commands with Examples
- File Permissions in Linux/Unix with Example
- Input Output Redirection in Linux/Unix Examples
- Pipe, Grep and Sort Command in Linux/Unix with Examples
- Linux Regular Expression Tutorial: Grep Regex Example

TCL Scripting Syllabus

- Introduction and Overview
- Tcl Syntax: quoting and substitution
- Expressions
- Variables: simple variables; associative arrays
- Lists; Keyed Lists
- Control Structures: built-ins
- Procedures; Recursion
- The Unix File System
- Files and I/O
- Strings
- Regular Expressions

- Writing Applications; Auto loading; Timing; Profiling
- Processes
- Error Handling; Defining Control Structures; Exceptions
- Client / Server; Distributed Programming
- Expect

Module-7: SYNTHESIS – ASIC DESIGN FLOW

- Introduction to ASIC's and ASIC flows
- Insight into various ASIC design Architecture
- Writing RTL for ASIC design flow
- ASIC Design Flow using Synopsys and cadence Tools
- Using special digital modules in ASIC design
- Static RAM and Dynamic RAM
- Clock and Reset managements, power sequencing
- Clock gating and low power designs
- Dedicated arithmetic functions

Module 8: STATIC TIMING ANALYSIS

- Introduction to STA
- Comparison with DTA
- Timing Path and Constraints
- Different types of clocks
- Clock domain and Variations
- Clock Distribution Networks
- How to fix timing failure
- Introductions to timing static and dynamic hazards,
- Path delay, Gate delay, Metastability states.
- Sequential timing delays like set-up time, hold time,
- Maximum frequency, violations, slew, slack.
- Delay analysis
- Sequential logic pad to set up,
- pad to pad,
- clk to next Reg,
- Reg to o/p and
- Reg to Reg. violations wrt sequential circuit.

Module-9: Low Power Design using UPF/CPF

- Low power techniques using clock gating to a design at the RTL and during synthesis
- Clock gating in multi-stage, hierarchical, low power designs
- Leakage power optimization using multi Vt standard cell libraries

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- Defining power intent using UPF for low power designs
- Understanding UPF 2.0 for better power optimization strategy
- Switchable & always on power domains.
- Level shifters, isolation requirements, retention logic
- Multi Voltage & Power Gating design during power planning in physical design
- Multi Voltage power mesh design for power islands.
- Floorplan and Placement requirements with multi voltage UPF design
- MCMM analysis with multi voltage power planning

Module-10: ASIC design standard cell libraries and flow setup

- Design data preparation and database creation,
- Process technologies and standard cell libraries.
- Understanding of standard cell technology parameters,
- netlist generation and technology mapping.
- Reviewing timing constraints and IO constraints.
- Low power and low area design concepts.

Module-11: Review synthesis principles and synthesis of design modules

- Implementation of RTL design and synthesis,
- generating netlist and estimating performance of synthesized design.
- Area/Timing/Power report checks,
- Design constraints for synthesis and defining Standard Design Constraints
- Efficient synthesis techniques. SDF generation

Module-12: Pre-Layout design partitioning and planning

- Design plan for hierarchical and flat design implementation,
- Better partition techniques and flow setup.
- Special cells and IO cells usage planning,
- Congestion removal techniques and implementation constraint setup.

Module-13: Design floor planning and power planning

- Understanding various floor planning techniques,
- Design Checks and Early performance Analysis
- Setting up guidelines for better floor planning and meeting design goals.
- IO PAD placement planning, power planning.
- Adding power rings and power mesh.
- PG Enhancements, PG DRC checks
- Pin planning and placement
- Time budgeting with annotated delays
- Macro floorplanning and placements

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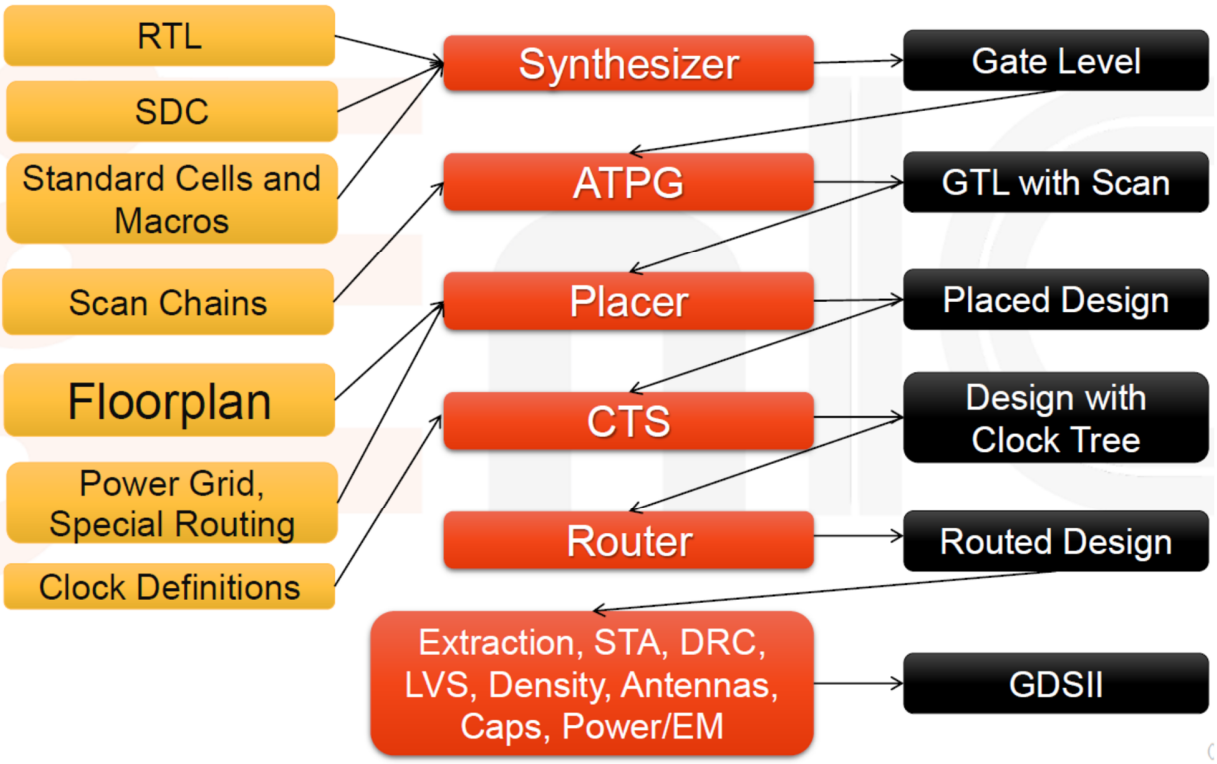
VLSI Physical Design Complete Flow Details



Module-14: Design Placement

- Design Placement requirements, pre-placement checks
- Various optimization techniques to avoid design congestion.
- Congestion driven design placement
- Performing timing analysis at various levels of floor planning.
- Pre and post placement optimization technique,
- setting up placement goals to meet design placement constraints,
- Fixing placement issues.

Module-15: Clock tree synthesis and timing analysis

- Implementation of clock tree in placed design.
- Implications of Clocking, analysis based timing, power, area and signal integrity
- Clock distribution in multi clocking designs.
- Clock Tree synthesis for Primary clocks and Generated clocks
- understanding various aspects of timing during CTS
- Parameters like clock setup/hold, skew and latency issues.
- Clock Tree Synthesis using EDA, CCOpt Methodology
- Adding buffers in clock tree and implementing clock tree.
- Analyzing timing reports after clock tree synthesis and fixing issues.

Module-16: Routing

- Understanding routing methodologies like trial route, special route, global routing and detailed routing.
- Multi layer routing and metal layer stacks
- Techniques to minimize wire-length, balance routing congestion
- Timing driven grid routing techniques
- Optimizing Critical paths
- Noise and SI driven routing
- Shielding Special nets
- Upsize driver or buffer
- Via Reduction
- Redundant via insertion
- Single vias vs multi-cut vias
- Incrimental routing for minimizing vias.
- Grouping wires in bussed routing.
- Tracks assignments for nets, pin to net routing
- Applying special routing rules
- Reduce cross coupling capacitance, wire widening to reduce resistance.
- Analyzing routed design checking post routed design issues,
- Solving DRC violations,
- Post route timing checks,
- Post route design optimization techniques

Module-17: Detailed timing analysis and optimizations, parasitic extraction

- Doing complete path and module based timing analysis,
- checking timing optimizer reports,
- Identifying failing paths, fixing issues.
- Extracting capacitor table values for the design.
- IR drop and electro migration analysis.

Module-18: Post route design checks and signoff

- Perform DRC,
- Logical Equivalence checking,
- generating detailed timing/power reports,
- Generating power reports.
- GDS-II generation.

Module-19: Project

1. Block Level Projects like, Leon processor, ARM11, Sparc Processor
2. SoC level full chip design, Leon SoC, RiSC SoC

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Prerequisites:

With Electronics major subject in B.E/B.Tech/M.E/M.Tech, atleast 60% throughout academic career Basic knowledge in Digital design.

Admission procedure:

Selection based on written test and personal Interviews. Syllabus for written test focused on Digital logic design, and Analytical and Logical questions. Outstanding performers will get special concessions in Fees. Working VLSI/Software professionals will get direct admissions.

Grading & Certifications

All the participants who fulfilled course assignments, projects, topic wise exams would be awarded with Course completion Certification

Placement Assistance

All the eligible candidates who have fulfilled requirements of the course will be given 100% placement assistance.

Duration:

6 months full time regular weekly & weekend batches

Course Fees:

Rs: 90,000 (Inc GST)